# Intelligent Fault Identification in Integrated Circuits Using Artificial Neural Network Models

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## Abstract

Ultra-high-density integrated circuits (ICs) with complex parasitic interdependencies and non-linear failure behaviors are the outcome of semiconductor technology's continual scaling into the deep sub-micron realm. A major diagnostic bottleneck results from the inability of rule-based automated test pattern generation (ATPG) and conventional deterministic diagnostic techniques to maintain accuracy in these fuzzy logic settings. In order to identify and localize intelligent faults in Very-Large-Scale Integration (VLSI) systems, a unique Multi-Stage Adaptive Back-Propagation Neural Network (MS-ABPNN) architecture is proposed in this research. The suggested model successfully separates structural and parametric flaws from background noise by using a dual-stage hidden processing block for feature extraction and non-linear mapping. According to results from experiments, the MS-ABPNN reduces diagnostic latency by 62.5% and achieves a defect localization accuracy of 97.6%, which is 9.4% better than typical neural models. The model's effectiveness as a reliable self-diagnostic framework for the upcoming generation of intelligent hardware and AI-specific accelerators is demonstrated by the incorporation of an adjustable learning rate, which guarantees quick convergence and great scalability.

## Keywords

VLSI, Fault Localization, MS-ABPNN, Deep Sub-Micron, ATPG, Adaptive Learning, IC Diagnostics, Parametric Defects, AI Accelerators.