Gate-Temperature-Controlled Thermal Transistor via Engineered Disorder in a Te-Doped W/MoS_2 Heterostructure

Samira Darbanhag
Department of Physics, Urmia University of Technology, Iran

Sohrab Behnia
Department of Physics, Urmia University of Technology, Iran

Fatheme Nemati
Department of Physics, Urmia University of Technology, Iran

Abstract:

This study presents a high-performance thermal transistor utilizing a Te-doped W/MoS_2 van der Waals heterostructure. By employing gate temperature (T_G) as the primary control parameter, the device achieves smooth n-to-p thermoelectric crossover and pronounced negative differential thermal resistance. A quantum-statistical framework based on the Brody parameter (β) is introduced to diagnose disorder and transport coherence, revealing that strategic Se doping in the MoS_2 channel regularizes phonon transport, while interfacial doping degrades performance. The transistor demonstrates an on-off ratio of ~100×, competitive with state-of-the-art solid-state thermal switches. These results establish gate-temperature tuning and disorder engineering as critical design principles for integrated thermal management, offering a pathway toward intelligent thermal circuits for next-generation computing and energy systems.

Thermal transistor, Gate-temperature tuning, Negative differential thermal resistance, Quantum chaos, Nanoelectronics thermal management.